4/13/10 cont'd

the size of the trigger element can be reduced.--.

IN THE CLAIMS:

Cancel claims 1-36.

Add the following new claims:

--37. (new) A semiconductor integrated circuit comprising:

a semiconductor substrate;

a CMOS inner circuit formed on said semiconductor substrate; and

an ESD protection circuit, connected between said CMOS inner circuit and a pad, for protecting said CMOS inner circuit against an overvoltage applied to said pad; wherein

said ESD protection circuit includes,

a vertical bipolar transistor formed on said semiconductor substrate and discharging an accumulated electric charge of said pad in a direction from a surface of said semiconductor substrate to a depth of said semiconductor substrate, and

a trigger element for switching on said vertical bipolar transistor when the overvoltage is applied to said paid.

--38. (new) The semiconductor integrated circuit according to claim 37, wherein a base and a collector of said vertical bipolar transistor are formed in a direction from a surface of said semiconductor substrate to a depth, and an emitter

of said vertical bipolar transistor is formed on the surface of said semiconductor substrate.

--39. (new) The semiconductor integrated circuit according to claim 37, wherein said trigger element includes a diode broken down by the overvoltage applied to said pad, and a resistor which increases a base potential of said vertical bipolar transistor by a trigger current accompanying to a breakdown of said diode.

--40. (new) The semiconductor integrated circuit according to claim 37, wherein said trigger element includes:

a diode which is formed with a semiconductor structure between a collector and a base of a vertical bipolar transistor having a same structure to that of said vertical bipolar transistor forming said ESD protection circuit, and is broken down by the overvoltage applied to said pad, and

a resistor which is connected between the base and a ground of said vertical bipolar transistor forming said diode, and increases a base potential of said vertical bipolar transistor forming said ESD protection circuit by a trigger current accompanying to a breakdown of said diode.

--41. (new) The semiconductor integrated circuit according to claim 39, wherein the diode of said trigger element is formed of a reverse diode.

--42. (new) The semiconductor integrated circuit according to claim 39, wherein the diode of said trigger element is formed of a forward diode.

--43. (new) The semiconductor integrated circuit according to claim 42, wherein said forward diode ensures a trigger voltage by connecting in multiple steps.

--44. (new) The semiconductor integrated circuit according to claim 37, wherein said pad may be an input terminal, an output terminal or an electric power source terminal.

--45. (new) The semiconductor integrated circuit according to claim 37, wherein

said ESD protection circuit includes a trigger element having first and second diodes and first and second resistors, and first and second vertical bipolar transistors of an NPN type;

a cathode of said first diode is connected with said pad and an anode of said first diode is connected with a base of said first vertical bipolar transistor;

a cathode of said second diode is connected with an electric power source terminal and an anode of said second diode is connected with a base of said second vertical bipolar transistor;

said first resistor is connected between the anode of said first diode and a ground terminal;

said second resistor is connected between the anode of said second diode and said pad;

a collector of said first vertical bipolar transistor is connected with said pad and an emitter of said first vertical bipolar transistor is connected with said ground terminal; and

a collector of said second vertical bipolar transistor

is connected with said electric power source terminal and an emitter of said second vertical bipolar transistor is connected with said pad.

--46. (new) The semiconductor integrated circuit according to claim 37, wherein

said ESD protection circuit includes a trigger element having first and second diodes and first and second resistors, and first and second vertical bipolar transistors of an PNP type;

a cathode of said first diode is connected with a base of said first vertical bipolar transistor and an anode of said first diode is connected with a ground terminal;

a cathode of said second diode is connected with a base of said second vertical bipolar transistor and an anode of said second diode is connected with said pad;

said first resistor is connected between the cathode of said first diode and said pad;

said second resistor is connected between the cathode of said second diode and said electric power source terminal;

a collector of said first vertical bipolar transistor is connected with said ground terminal and an emitter of said first vertical bipolar transistor is connected with said pad; and

a collector of said second vertical bipolar transistor is connected with said pad and an emitter of said second vertical bipolar transistor is connected with said electric power source terminal.

--47. (new) The semiconductor integrated circuit

according to claim 39, wherein

said vertical bipolar transistor is an NPN type;

the cathode of said diode is connected with said pad and the anode of said diode is connected with the base of said vertical bipolar transistor;

a resistor is connected between the anode of said diode and a ground terminal; and

the collector of said vertical bipolar transistor is connected with said pad and the emitter of said vertical bipolar transistor is connected with said ground terminal.

--48. (new) The semiconductor integrated circuit according to claim 39, wherein

said pad is an electric power terminal;

said vertical bipolar transistor is of PNP type;

a cathode of said diode is connected with a base of said vertical bipolar transistor and an anode of said diode is connected with a ground terminal;

a resistor is connected between the cathode of said diode and said electric power terminal; and

a collector of said vertical bipolar transistor is connected with said ground terminal and an emitter of said vertical bipolar transistor is connected with said pad.

--49. (new) The semiconductor integrated circuit according to claim 37, wherein

said ESD protection circuit includes a trigger element having first and second diodes and first and second resistors, and

first and second vertical bipolar transistors of an NPN type;

an anode of said first diode is connected with said pad and a cathode of said first diode is connected with a base of said first vertical bipolar transistor;

an anode of said second diode is connected with an electric power source terminal and a cathode of said second diode is connected with a base of said second vertical bipolar transistor;

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said first resistor is connected between the cathode of said first diode and the ground terminal;

said second resistor is connected between the cathode of said second diode and said pad;

a collector of said first vertical bipolar transistor is connected with said pad and an emitter of said first vertical bipolar transistor is connected with said ground terminal; and

a collector of said second vertical bipolar transistor is connected with said electric power source terminal and an emitter of said second vertical bipolar transistor is connected with said pad.

--50. (new) The semiconductor integrated circuit according to claim 37, wherein

said ESD protection circuit includes a trigger element having first and second diodes and first and second resistors, and first and second vertical bipolar transistors of a PNP type;

an anode of said first diode is connected with a base of said first vertical bipolar transistor and a cathode of said first

diode is connected with a ground terminal;

an anode of said second diode is connected with a base of said second vertical bipolar transistor and a cathode of said second diode is connected with said pad;

said first resistor is connected between the anode of said first diode and said pad;

said second resistor is connected between the anode of said second diode and said electric power source terminal;

the collector of said first vertical bipolar transistor is connected with said ground terminal and the emitter of said first vertical bipolar transistor is connected with said pad; and

the collector of said second vertical bipolar transistor is connected with said pad and the emitter of said second vertical bipolar transistor is connected with said electric power source terminal.

--51. (new) The semiconductor integrated circuit according to claim 39, wherein

said vertical bipolar transistor is of an NPN type;

an anode of said diode is connected with said pad and a cathode of said diode is connected with a base of said vertical bipolar transistor;

a resistor is connected between the cathode of said diode and a ground terminal; and

a collector of said vertical bipolar transistor is connected with said pad and an emitter of said vertical bipolar transistor is connected with said ground terminal.

--52. (new) The semiconductor integrated circuit according to claim 39, wherein

said vertical bipolar transistor is of a PNP type;

an anode of said diode is connected with a base of said vertical bipolar transistor and a cathode of said diode is connected with a ground terminal;

a resistor is connected between the anode of said diode and said electric power source terminal; and

a collector of said vertical bipolar transistor is connected with said ground terminal and an emitter of said vertical bipolar transistor is connected with said pad.

--53. (new) The semiconductor integrated circuit according to claim 40, wherein

said vertical bipolar transistor forming said diode of said trigger element is an NPN type vertical bipolar transistor A and an NPN type vertical bipolar transistor B, and said resistor is a first and a second resistor;

a plurality of said pads are provided;

the vertical bipolar transistor of said ESD protection element is an NPN type vertical bipolar transistor C and an NPN type vertical bipolar transistor D acting as said second vertical bipolar transistor;

collectors of said vertical bipolar transistors A, C are connected with said pads, bases thereof are connected with each other and emitters thereof are connected with a ground terminal;

said first resistor is connected between the bases of

said vertical bipolar transistors A, C and said ground terminal;

collectors of said vertical bipolar transistors B, D are connected with an electric power source terminal, bases thereof are connected with each other and emitters thereof are connected with said pads; and

said second resistor is connected between the bases of said vertical bipolar transistors B, D and said pads.

--54. (new) The semiconductor integrated circuit according to claim 40, wherein

the vertical bipolar transistor of said diode and the vertical bipolar transistor of said ESD protection circuit are NPN type, and their collectors are connected with said pad and their bases are connected with each other and their emitters are connected with a ground terminal; and

a resistor is connected between the bases of said two vertical bipolar transistors and the ground terminal.

--55. (new) The semiconductor integrated circuit according to claim 40, wherein

said ESD protection circuit includes a PNP type vertical bipolar transistor A and a PNP type vertical bipolar transistor B forming said diode, a trigger element having a first and a second resistor, and a PNP type vertical bipolar transistor C and a PNP type vertical bipolar transistor D;

emitters of said bipolar transistors A, C are connected with said pads, bases thereof are connected with each other and collectors thereof are connected with a ground terminal;

said first resistor is connected between the bases of said vertical bipolar transistors A, C and said pads;

emitters of said vertical bipolar transistors B, D are connected with an electric power source terminal, bases thereof are connected with each other and collectors thereof are connected with said pads; and

said second resistor is connected between the bases of said vertical bipolar transistors B, D and said electric power source terminal.

--56. (new) The semiconductor integrated circuit according to claim 40, wherein

the vertical bipolar transistor forming said diode of said trigger element and the vertical bipolar transistor of said ESD protection circuit are of a PNP type, and collectors thereof are connected with a ground terminal, bases thereof are connected with each other and emitters thereof are connected with said pads; and

resistors are connected between the bases of said two vertical bipolar transistors and said pads.

--57. (new) The semiconductor integrated circuit according to claim 40, wherein the vertical bipolar transistor forming the diode of said trigger element and the vertical bipolar transistor of said ESD protection circuit are structured to have a common collector layer.

--58. (new) The semiconductor integrated circuit according to claim 37, wherein one of said vertical bipolar

transistor and said diode comprises, at least one of: a first N^- type well formed on a P type silicon substrate surface; a second N^-type well adjacent to the first N^-type well and formed on said P type silicon substrate surface; a second N^+layer formed on the second N-type well surface; a P^-type well formed on said first N^- type well surface; a P^+layer and a first N^+layer formed on the P^- type well surface apart from each other; and an insulation material installed between the P^+layer and the first N^+layer for preventing an electric connection with said P+$^+$layer and the first N^+layer, and

said second N^-type well and said P^-type well are insulated by the insulation material for isolation, and said P type silicon substrate and said P^-type well are insulated by the insulation material for isolation.

--59. (new) The semiconductor integrated circuit according to claim 37, wherein one of said vertical bipolar transistor or said diode comprises, at least one of: a first P^- type well formed on a N type silicon substrate surface; a second P^-type well adjacent to the first P^-type well and formed on said N type silicon substrate surface; a second P^+layer formed on this second P^-type well surface; a N^-type well formed on said first P^- type well surface; a N^+layer and a first P^+layer formed on the N^- type well surface apart from each other; and an insulation material installed between the N^+layer and the first P^+layer for preventing the electric connection with said P^+layer and first N^+layer, and

said second P^-type well and said N^-type well are insulated by the insulation material for isolation, and said N type silicon substrate and said N^-type well are insulated by the insulation material for isolation.

--60. (new) The semiconductor integrated circuit according to claim 58, wherein said insulation material is one of a dummy gate electrode and a simple insulation film.

--61. (new) The semiconductor integrated circuit according to claim 60, wherein said dummy gate electrode or said insulation film is formed in a ring shape on said silicon substrate surface.

--62. (new) The semiconductor integrated circuit according to claim 37,

wherein said diode comprises: an N^-type well formed on a P type silicon substrate surface; a P^+layer and an N^+layer formed on the N^-type well surface apart from each other; and an insulation material formed inside from said P type silicon substrate surface between the P^+layer and N^+layer.

--63. (new) The semiconductor integrated circuit according to claim 37,

wherein said diode comprises: a P^-type well formed on an N type silicon substrate surface; a P^+layer and an N^+layer formed on the P^-type well surface apart from each other; and an insulation material formed inside from said P type silicon substrate surface between the P^+layer and N^+layer.

--64. (new) The semiconductor integrated circuit

according to claim 37,

wherein said diode comprises: an N^-type well formed on a P type silicon substrate surface; a P^-type well formed on the N^- type well surface; a P^+layer and N^+layer formed on the P^-type well surface apart from each other; and an insulation material installed on said P type silicon substrate surface between the P^+layer and N^+layer for preventing electric connection between said P^+layer and N^+layer, and

said P type silicon substrate and said P^-type well are insulated by the insulation material for isolation.

--65. (new) The semiconductor integrated circuit according to claim 37,

wherein said diode comprises: a P^-type well formed on an N type silicon substrate surface; an N^-type well formed on the P^- type well surface; a P^+layer and N^+layer formed on the N^-type well surface apart from each other; and an insulation material installed on said N type silicon substrate surface between the P^+layer and N^+layer for preventing electric connection between said P^+layer and N^+layer, and

said N type silicon substrate and said N^-type well are insulated by the insulation material for isolation.

--66. (new) The semiconductor integrated circuit according to claim 37,

wherein said diode comprises: a P^-type well formed on a silicon substrate surface; N^+layer and the P^+layer formed on the P^- type well surface apart from each other; and a dummy gate

electrode installed on said P^-type well between the N^+layer and P^+layer through an insulation film and connected with a ground terminal.

--67. (new) The semiconductor integrated circuit according to claim 37,

wherein said diode comprises: a N^-type well formed on a silicon substrate surface; N^+layer and the P^+layer formed on the N^- type well surface apart from each other; and a dummy gate electrode installed on said N^-type well between the N^+layer and P^+layer through an insulation film and connected with a ground terminal.

--68. (new) A method for fabricating a semiconductor integrated circuit comprising:

a first step of simultaneously forming an N^- type well of a CMOS transistor comprising an inner circuit and an N^- type well for collector connection to be connected with a collector of a vertical bipolar transistor on a P type silicon substrate;

a second step of simultaneously forming a collector N^- type well to be a collector of said vertical bipolar transistor and an N^- type well of a diode on said P type silicon substrate;

a third step of simultaneously forming a P^- type layer to be a base in the collector N^- type well of said vertical bipolar transistor and a P^- type layer to be an anode in the N^- type well of said diode;

a fourth step of simultaneously forming an N^+ type layer in the P^- type well of said CMOS transistor, an N^+ type layer in

the N^- type well for collector connection of said vertical bipolar transistor, an N^+ type layer to be an emitter in the P^- type layer of said vertical bipolar transistor, and an N^+ type layer to be a cathode in the P^- type layer of said diode; and

a fifth step of simultaneously forming a P^+ type layer on the N^- type well of said CMOS transistor, a P^+ type layer on the P^- type layer of said vertical bipolar transistor, and a P^+ type layer on the P^- type layer of said diode.

--69. (new) A method for fabricating a semiconductor integrated circuit comprising:

a first step of simultaneously forming an N^-type well of a CMOS transistor constituting an inner circuit and an N^-type well for collector connection to be connected with a vertical bipolar transistor on a P type silicon substrate;

a second step of simultaneously forming a collector N^- type well to be a collector of said vertical bipolar transistor and the N^-type well of a diode on said P type silicon substrate;

a third step of simultaneously forming a P^-type layer to be a base in the collector N^-type well of said vertical bipolar transistor and the P^-type layer to be a cathode in the N^-type well of said diode;

a fourth step of simultaneously forming an N^+layer in the P^-type well of said CMOS transistor, the N^+layer in the N^-type well for collector connection of said vertical bipolar transistor, the N^+layer to be an emitter in the P^-type layer of said vertical bipolar transistor, and the N^+layer to be an anode in the P^-type

layer of said diode; and

a fifth step of simultaneously forming the P^+layer in the N^-type well of said CMOS transistor, the P^+layer in the P^-type layer of said vertical bipolar transistor and the P^+layer in the P^-type layer of said diode.

--70. (new) The method for fabricating the semiconductor integrated circuit according to claim 68, further comprising a step of forming a dummy gate electrode simultaneously with a gate electrode of said CMOS transistor in the region where the collector N^- type well of said vertical bipolar transistor and N^- type well of said diode are formed in said second step, wherein said dummy gate electrode is to prevent connection in the subsequent steps between the N^+ type layers of said vertical bipolar transistor and said diode formed in said fourth step and the P^+ type layers of said vertical bipolar transistor and said diode formed in the fifth step.

--71. (new) The method for fabricating the semiconductor integrated circuit according to claim 68, further comprising a step of forming an insulation layer which prevents connection in the subsequent steps between the N^+ type layers of said vertical bipolar transistor and said diode formed in said fourth step and the P^+ type layers of said vertical bipolar transistor and said diode formed in the fifth step.